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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/050,004	01/14/2002	Mian Smith	015114-054000US	5525

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 02/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/050,004	SMITH ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "programmable logic circuitry" (claim 29) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 29 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification fails to teach "a programmable logic circuitry".

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 20 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 20 is misdescriptive and renders the claim indefinite. It is misdescriptive for reciting "coupling a gate and a drain/source of the first transistor through a fifth transistor in response to the first clock signal" and "coupling a gate and a drain/source of the second transistor through a sixth transistor in response to the second clock signal". Figure 4 shows the second clock (VCK1) signal is for coupling the gate and drain/source of first transistor 402 through the fifth transistor 442, and the first clock signal (VLK3) signal is for coupling the gate and drain/source of second transistor 403 through the sixth transistor 443.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-3, 12-13, 19, 21 and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Muramoto (JP 61-254078).

As to claim 1 and 29, Muramoto discloses in figure 1 a charge pump circuit, and a method thereof, comprising: a first transistor (last transistor in the front state 4); a first capacitor coupled to the first transistor (last capacitor in the front state 4); a second transistor (first transistor in the rear state 5) coupled to the first transistor; and a second capacitor (first capacitor in the rear state 5) coupled to the second transistor, wherein the second transistor has a lower threshold voltage than the first transistor at a common source voltage (abstract, the transistors in the rear state 5 are depletion type transistors which have lower threshold voltages than transistors

in the front state 4). As further called for claim 29, it is inherent for the system having a programmable logic circuitry.

As to claim 2, figure 1 further shows a third transistor (middle transistor in the rear state 5) coupled to the second transistor; and a third capacitor (middle capacitor in the rear state 5) coupled to the third transistor, wherein the third transistor has a lower threshold voltage than the first transistor at a common source voltage.

As to claim 3, figure 1 shows a fourth transistor (last transistor in the rear state 5) coupled to the third transistor; and a fourth capacitor (the last capacitor in the rear state 5) coupled to the fourth transistor, wherein the fourth transistor has a lower threshold voltage than the first transistor at a common source voltage.

As to claim 10, Muramoto's figure 1 shows the first and third capacitors are coupled to receive a first clock signal (1), and the second and fourth capacitors are coupled to receive a second clock signal (2).

Claims 12, 13 and 19 recite a method having similar limitations of claims 1-3 and 10. Therefore, they are rejection for the same reasons.

As to claim 21, figure 1 shows a charge pump circuit comprising a first stage (first transistor in the rear stage 5) comprising a first depletion field effect transistor; a second stage (middle transistor in the rear stage 5) comprising a second depletion field effect transistor, the second state being coupled to the first stage; a first capacitor (first capacitor) coupled to the first stage; and a second capacitor coupled to the second stage.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 4, 6-9, 14-18, 22-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muramoto (JP 61-254078).

As to claims 4, 6-9 and 14-18, Mamoto's figure 1 shows all limitations of the claim except for fifth, sixth, seventh, eighth, ninth, tenth, eleventh, twelfth, thirteenth, fourteenth, and fifteenth transistors coupled in series to the fourth transistor; and fifth, sixth, seventh, eighth, ninth, tenth, eleventh, twelfth, thirteenth, fourteenth, and fifteenth capacitors coupled to the fifth, sixth, seventh, eighth, ninth, tenth, eleventh, twelfth, thirteenth, fourteenth, and fifteenth transistors, wherein the fifth, sixth, seventh, eighth, ninth, tenth, eleventh, twelfth, thirteenth, fourteenth, and fifteenth transistors have lower threshold voltage than the first transistor at a common source voltage. However, it is well known in the art that the more charge pump units (capacitor and diode connected transistor) connected in series, the higher the output voltage level. Therefore, it would have been obvious to one having ordinary skill in the art to add more charge pump unit(s) such as fifth, sixth, seventh...fifteenth...etc. transistors and fifth, sixth, seventh, eighth...fifteenth...etc. capacitors for the purpose of increasing the output voltage level.

Claims 14-18 recite a method having similar limitations of claims 4 and 6-9. Therefore, they are rejected for the same reasons.

As to claims 22-25, figure 1 shows all limitations of the claims except for third, fourth, fifth...eleventh stages (depletion transistors) coupled in series and third, fourth, ...eleventh capacitors respectively coupled to the third, fourth, ...eleventh stages. . However, it is well known in the art that the more charge pump units (capacitor and diode connected transistor) connected in series, the higher the output voltage level. Therefore, it would have been obvious to one having ordinary skill in the art to add more charge pump unit(s) such as fourth, sixth, seventh...fifteenth...etc. transistors and fourth, sixth, seventh, eighth...fifteenth...etc. capacitors for the purpose of increasing the output voltage level.

As to claim 26, it is inherent that the first and third capacitors coupled to receive a first clock signal, and the second and fourth capacitors are coupled to receive a second clock signal.

10. Claims 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (USP 5978283) (Applicant's ISD) in view of Muramoto (JP 61-254078).

Hsu et al's figure 1 shows a charge pump circuit having plurality of transistors (A1-A8) connected in series; plurality of capacitors (C1-C8) respectively connected to the plurality of transistors (A1-A8); and plurality of diode connected transistors (M1-M8) respectively connected to the gate of the plurality of transistors (A1-A8). Thus, figure 1 shows all limitations of the claim except for at least the last three transistors in the plurality of transistors having threshold voltage lower than the threshold voltage of the rest of transistors. However, Muramoto's figure 1 teaches the more type threshold voltages of MOS transistors are effectively used to obtain a higher output voltage. Therefore, it would have been obvious to one having ordinary skill in the art to make at least the last three transistors of Hsu et al. to have lower

threshold voltage than the rest of the transistors for the purpose of generating higher output voltage.

11. Claims 11, 20, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukui (USP 6157242) in view of Muramoto (JP 61-254078).

As to claims 11, 20 and 27, Fukui's figure 3 shows a charge pump circuit, and method thereof, having first to fourth transistors (N2s in stg3-stg6) coupled in series, first to fourth capacitors (C2s in stg2-stg5) respectively coupled to the first to fourth transistors, wherein the first and third capacitors are coupled to receive a first clock signal (CLK4), and the second and fourth capacitors are coupled to receive a second clock signal (CKL2); a fifth capacitor (C1 in stg3) coupled to the first transistor and a third clock signal (CLK1); a sixth capacitor (C1 in stg4) coupled to the second transistor and a fourth clock signal (CLK3); a seventh capacitor (C1 in stg5) coupled to the third transistor and the third clock signal (CLK1); and an eighth capacitor (C1 in stg6) coupled to the fourth transistor and the fourth clock signal (CLK3). Thus, figure 3 shows all limitations of the claim except for the second to fourth transistors having lower threshold voltage than the first transistors. However, Muramoto's figure 1 teaches the more type threshold voltages of MOS transistors are effectively used to obtain a higher output voltage. Therefore, it would have been obvious to one having ordinary skill in the art to make at least transistors N2 in stg4-stg8 to have lower threshold voltage than the rest of the transistors for the purpose of generating higher output voltage (the selection of the number of low threshold voltage transistor is seen as an obvious design choice depending upon the desire output level). As further called for claim 27, the second to fifth transistors, wherein the fifth transistor is transistor in stg7, are now the first to fourth transistors.

As to claim 28, Fuk.'s figure 3 shows fifth, sixth, seventh and eighth transistors (N1s in stg4 – stg7).

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 703-308-6174. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

QT

QT
February 5, 2003

TIMOTHY P. CALLAHAN
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